PATENT
Attorney Docket No.: 10018224-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	Blaine D. Gaither, et al.	Examiner	Henry Tsai
Serial No.	10/002,971	Group Art No.	2183
Filed	October 26, 2001	Confirmation No.	3480
For	Method Of Optimization Of CPU And Chipset Performance By Support Of Optional Reads By CPU And Chipset		

April 4, 2005

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

In accord with 37 C.F.R. § 41.37, and fully responsive to the Office Action of November 17, 2004, Appellants hereby file their appeal brief in support of their Appeal in the above-identified matter (hereinafter the '971 Application). A notice of appeal, with appropriate fee of $500 as required by 37 C.F.R. §§41.31, 41.20(b)(1), was filed on February 17, 2004. Three copies of this brief are enclosed. The $500 fee for this appeal brief, as required by 37 C.F.R. §41.20(b)(2), is also filed herewith. This appeal brief is timely filed within two months of the mailing of the notice of appeal.

04/07/2005 MAHMED1 00000016 082025 10002971
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(1) **Real party in interest.**

The real party in interest for this appeal is Hewlett-Packard Development Company, L.P. (HPDC), a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, L.L.C. Evidence of this assignment, which was recorded on September 30, 2003, may be found at reel/frame 014061/0492.

(2) **Related appeals and interferences.**

No other appeals or interferences are currently known to Appellant that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

(3) **Status of claims.**

Claims 1-19 are pending in the '971 Application. Applicants appeal all claims 1-19. Claims 1-19 now stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,567,901 ("Neufeld '901"), also owned by the HPDC.

(4) **Status of amendments.**

The '971 Application was filed on October 26, 2001. A first office action was mailed on June 29, 2004, to which a response was filed and entered September 29, 2004. On November 17, 2004, a final office action was mailed, prompting this appeal. Claims 1-19 are currently pending, of which claims 11-12 and 19 are original (without claim amendment during prosecution). Claims 1-10 and 13-18 were amended in the response of September 29, 2004.

(5) **Summary of claimed subject matter.**

The inventions of claims 1-13 relate to a method for processing a memory access request within processing architecture. The flowchart 200 of FIG. 3 illustrates exemplary processing of an instruction (e.g., a memory access request

such as illustrated as instruction 100, FIG. 2) through architecture (e.g., architecture 10, FIG. 1). The method of claim 1 is also understood in connection with paragraphs [0005]-[0006], [0008]-[0010], [0012]-[0017] of the specification. In particular, a determination is made whether the memory access request is speculative or not. See, e.g., paragraphs [0005]-[0006], [0012], [0032] of the specification. If the request is speculative, an assessment is made of interconnect and target resource conditions. See, e.g., paragraph [0016] for target resource conditions (e.g., memory utilization, memory congestion, buffer space utilization and bus congestion) and paragraph [0017] for interconnect conditions (e.g., bus utilization, bus congestion, crossbar utilization, crossbar congestion and point to point link utilization). The memory request is then processed, or not, based on the conditions. See, e.g., paragraph [0032] of the specification. The inventions of claims 14-15 relate to a CPU architecture that initiates both speculative and non-speculative memory access requests. Such CPU architecture is for example architecture 10, FIG. 1. The inventive features of the CPU architecture include decode logic, to determine whether memory access requests are speculative or not, and assessment logic, to determine one or both of interconnect and target resource conditions. See, e.g., paragraphs [0007], [0015], [0018], [0027]-[0029] and FIG. 1 of the specification. The inventions of claims 16-19 relate to a system for processing speculative memory access requests within a processing architecture (e.g., architecture 10, FIG. 1). The system includes memory access requests (e.g., such as shown in FIG. 2), and decode and processing logic (e.g., such as discussed in paragraphs [0027]-[0029] of the specification; see also FIG. 1), to determine the speculative nature of the memory requests and to process the requests depending on the target resource and/or interconnect conditions.

(6) Grounds for rejection to be reviewed on appeal.

A. Whether claims 1-13 are anticipated by U.S. Patent No. 6,567,901 ("Neufeld '901") in accordance 35 U.S.C. §102(e).

B. Whether claims 14-15 are anticipated by Neufeld '901 in accordance 35 U.S.C. §102(e).

C. Whether claims 16-19 are anticipated by Neufeld '901 in accordance 35 U.S.C. §102(e).

(7) **Argument.**

Argument A

Neufeld '901 does not teach or suggest each and every claim limitation within claims 1-13 as required by 35 U.S.C. § 102(e).

To anticipate a claim, Neufeld '901 must teach every element of the claim and "the identical invention must be shown in as complete detail as contained in the ... claim." *MPEP 2131* citing *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987) and *Richardson v. Suzuki Motor Co.*, 868 F2.d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989). Neufeld '901 does not teach every element of claims 1-19.

Neufeld '901 discloses a system with read around speculative load. However, in the system of Neufeld '901, the decision to cancel a request, or to upgrade speculative requests to non-speculative, is made by the processor, and depends upon the execution path of the processor through software. For example, Neufeld '901 discloses (see col 5, lines 60-62): '...the processor 30 might pause the application 451 and issue another memory request 421 to shorten the delay.' Similarly, Neufeld '901 further discloses (see col 5 lines 65-67, col 6 lines 1-2): 'If the processor 30 reaches a point where it realizes that it is not going to need memory request 421, the processor 30 would generate a memory request indicating that the memory request 421 may be cancelled.' The Neufeld '901 processor thus determines and initiates the modification of the status of memory requests. Neufeld '901 does not disclose a system whereby one or both of interconnect and target resource conditions are used to determine if a speculative memory request is processed, or not, as in each independent claim (claims 1, 14 and 16) of the '971 Application.

More particularly, the '971 Application teaches the handling of speculative memory access requests (e.g., memory access requests that are predicted by prefetch unit 26 of processor 12, as for example shown in FIG. 1). The '971 Application also teaches assessing conditions of the interconnect and target resources to determine if a

speculative memory access will be processed, delayed or aborted. See, e.g., the '971 Application, paragraph [0007].

Claim 1

Accordingly, claim 1 recites a method for processing a memory access request within a processing architecture, and requires the steps of:

a) determining whether the memory access request is speculative or not based upon a first identifier;

b) assessing one or both of interconnect and target resource conditions in the event that the memory access request is speculative; and

c) either processing the memory access request, or not, as a function of the conditions.

In step b), claim 1 specifically requires that one or both of the interconnect and target resource conditions are assessed to determine if a speculative memory access request is processed. Neufeld '901 does not – anywhere - teach or suggest this feature. Instead, Neufeld '901 specifically discloses (col. 5, line 65 – col. 6, line 2) that the processor "...realizes that it is not going to need a memory request 421, the processor 30 would generate a memory request indicating that the memory request 421 may be cancelled." Thus, in Neufeld '901, a speculative request 421 may only be cancelled by the processor 30; whereas, in the '971 Application, the assessment step may abort a speculative memory access if resource conditions so dictate.

The Examiner argues that the memory request processing logic of Neufeld '901 assesses (or checks) the target resource condition in order to complete the speculative memory request 421. However, this assessment is by protocol and does not determine if 'traffic on bus 30 is too congested' or that 'target memory ... is saturated' - as in the '971 Application. Such a protocol does not therefore include assessing and processing steps that may postpone or abort processing of a speculative memory request, as in claim 1.

Accordingly, claim 1 is not anticipated by Neufeld '901.

Claims 2 through 13 depend from claim 1, and benefit from like arguments. Specifically, these arguments hereinabove clearly show that Neufeld '901 does not teach each and every element of claim 1 and that, therefore, Neufeld '901 cannot also

teach the elements of claims 2-13. But in the context of claim 1, these claims have additional reasons for patentability.

Claim 2

- Amended claim 2 recites decoding the first identifier as a first bit field within the memory access request. Neufeld '901 does not disclose or suggest such features.

Claim 3

- Amended claim 3 recites encoding the first bit field within the memory access request to define a speculative ID of the memory access request. Neufeld '901 does not disclose or suggest such features.

Claim 4

- Amended claim 4 recites that the memory access request includes one of an instruction, a message and an operational request. Neufeld '901 does not disclose or suggest such features.

Claim 5

- Amended claim 5 recites determining a priority of the memory access request based upon a second identifier, in the event that the memory access request is speculative, and processing the memory access request, or not, based upon the conditions and the priority. Neufeld '901 does not disclose or suggest such features.

Claim 6

- Amended claim 6 recites determining a priority by decoding the second identifier as a second bit field within the memory access request. Neufeld '901 does not disclose or suggest such features.

Claim 7

- Amended claim 7 recites encoding the second bit field within the memory access request to define a priority of the memory access request. Neufeld '901 does not disclose or suggest such features.

Claim 8

- Amended claim 8 recites that the memory access request includes one of a memory read request and a memory load request. Neufeld '901 does not disclose or suggest such features.

Claim 9

- Amended claim 9 recites utilizing one of a CPU, chipset and memory controller to determine whether the memory access request is speculative. Neufeld '901 does not disclose or suggest such features.

Claims 2-9 are thus also not anticipated by Neufeld '901.

Claim 10

Further, amended claim 10 recites that at least one of the CPU, chipset and memory controller independently controls the step of processing the memory access request based on the conditions. Neufeld '901 does not teach of processing the memory access request based on such conditions. Neufeld '901 discloses, instead, that a system prioritizes requests, giving priority to non-speculative requests; but it does not teach that conditions (traffic and congestion) of the interconnect and the target resource are used during processing of a memory access request. Neufeld '901 also does not consider bus traffic and target resource congestion. The use of a communication protocol on a bus cannot reasonably anticipate the assessment of bus traffic conditions or target resource congestion as described in the '971 Application. In Neufeld '901, processor 30 modifies the status of a speculative request based upon execution of the application 451. See Neufeld '901, col. 5, lines 56-62, and col. 5 line 65 through col. 6 line 2. Accordingly, Neufeld '901 does not, and cannot, teach every element of claim 10.

Claim 11

Claim 11 recites that the step of assessing target resource conditions includes assessing one or more of memory utilization, memory congestion, buffer space utilization, and bus congestion. Neufeld '901 does not disclose or suggest such features.

Claim 12

Claim 12 recites that the step of assessing interconnect conditions includes assessing one or more of bus utilization, bus congestion, crossbar utilization, cross bar congestion, and point to point link utilization. As noted above, Neufeld '901 does not teach of monitoring memory utilization, memory congestion, buffer space utilization or bus congestion. Accordingly, Neufeld '901 does not, again, anticipate claim 12.

Claim 13

Amended claim 13 recites the step of notifying one or more logic devices when the memory access request is not processed. Accordingly, the determination of whether the memory access request is processed, or not, may be made external to the processor, wherein the processor is informed if the speculative memory access request is aborted.

Neufeld '901, on the other hand, discloses that the processor determines if a request is deleted, based upon algorithm execution. According to Neufeld '901, a first speculative request is issued to the memory controller, and, later, the processor may send a second request to inform the memory controller not to process the first speculative request. Unlike Neufeld '901, in claim 13 the determination to process or abort a speculative memory access request may be made by the memory controller, for example. If the memory controller determines that the speculative memory access request is to be aborted, the memory controller sends notification of the aborted speculative memory access request to the processor.

Neufeld '901 does not, again, anticipate claim 13.

Argument B

Neufeld '901 does not teach or suggest each and every claim limitation within claims 14-15 as required by 35 U.S.C. § 102(e).

Claim 14

Claim 14 recites CPU architecture that initiates both speculative and non-speculative memory access requests, an improvement comprising decode logic for determining whether the memory access requests are speculative, and assessment logic for determining one or both of interconnect and target resource conditions, the

CPU architecture processing speculative memory access requests, or not, as a function of the conditions. The assessment logic of claim 14 may therefore assess the condition of the interconnect or target resource. As argued above, Neufeld '901 does not teach utilizing conditions of the interconnect or target resource.

With regard to claim 14, the Examiner again contends that '...assessing target resource condition is an inherent step.' We respectfully disagree. A bus protocol may utilize control signals to correctly sequence data transfer to and from a resource; however, such a protocol does not assess 'conditions' of the resource as required by claim 14. See also the '971 Application, paragraphs [0012], [0031] and [0032]. Accordingly, the assessment logic may determine if a speculative memory request will be processed, or not, based upon the 'condition' of the memory resource and independent of any decision by the processor. Accordingly, as in other claims, Neufeld '901 does not teach or suggest claim 14; it cannot therefore anticipate claim 14.

Claim 15

Claim 15 depends from claim 14 and benefits from like arguments. But claim 15 further recites a prefetch unit (see FIG. 1) that prefetches memory access requests so that the assessment logic can assess whether it is speculative or not. Neufeld '901 also does not disclose features of claim 15 in the context of independent claim 14; Neufeld '901 thus cannot anticipate claim 15 either.

Argument C

Neufeld '901 does not teach or suggest each and every claim limitation within claims 16-19 as required by 35 U.S.C. § 102(e).

Claim 16

Claim 16 recites a system for processing speculative memory access requests, comprising: one or more memory access requests having a bit field defining the memory access requests as speculative or non-speculative; decode logic for decoding the bit field to determine whether one or more memory access requests are speculative; and processing logic for processing speculative memory access requests, or not, based on at least one of interconnect and target resource conditions.

As previously argued above, Neufeld '901 does not teach or suggest processing logic for processing speculative requests, or not, based on at least one of interconnect and target resource conditions. We disagree, again, with the Examiner's statement that 'assessing target resource condition is an inherent step.' In prior communications with the Examiner, we have requested evidence pursuant to MPEP §2144 that supports the Examiner's contention of this inherent step; such evidence has never been provided to us. We on the other hand contend that assessing the target resource or the interconnect condition to determine if the target resource is saturated, or if the interconnect is congested [see, e.g., the '971 Application, paragraph [0031]], is not inherent to processing speculative requests as disclosed by Neufeld '901. Neufeld '901 does not, again, anticipate claim 16.

Claims 17-19 depend from claim 16 and benefit from like arguments. But these claims have additional reasons that patentably distinguish over Neufeld '901.

Claim 17

For example, in amended claim 17, one or both of the decode logic and processing logic are located within a CPU, a chipset, a bus controller or a memory controller. Neufeld '901 simply does not teach or disclose – anywhere - such decode and processing logic.

Claim 18

In claim 18, memory access requests comprise memory read instructions. In the context of claim 16, claim 18 too is not disclosed or taught by Neufeld '901.

Claim 19

Claim 19 recites a bus controller for assessing one or more of bus congestion and bus utilization conditions. Neufeld '901 does not teach assessing bus congestion and bus utilization conditions for purposes of determining if speculative requests are processed or not. Claim 19 is therefore not anticipated by Neufeld '901.

(8) Claims appendix.

Appellants enclose a copy of the claims involved in this appeal as an appendix hereto.

(9) Evidence appendix.

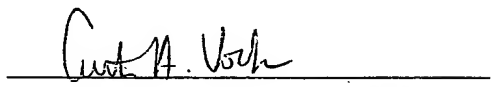
Not applicable.

(10) Related proceedings appendix.

Not applicable.

Other than the costs for this appeal brief, no further fees are deemed due in connection with this matter. However, the Commissioner is hereby authorized to charge any fees which may be due in this matter from Deposit Account Number 08-2025.

Respectfully submitted,
LATHROP & GAGE LC

By: 

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APPENDIX TO APPEAL BRIEF

1. (Previously Presented) A method for processing a memory access request within processing architecture, comprising the steps of: determining whether the memory access request is speculative or not based upon a first identifier; assessing one or both of interconnect and target resource conditions in the event that the memory access request is speculative; and either processing the memory access request, or not, as a function of the conditions.

2. (Previously Presented) The method of claim 1, wherein the step of determining whether the memory access request is speculative comprises decoding the first identifier as a first bit field within the memory access request.

3. (Previously Presented) The method of claim 2, further comprising encoding the first bit field within the memory access request to define a speculative ID of the memory access request.

4. (Previously Presented) The method of claim 1, wherein the memory access request comprises one of an instruction, a message and an operational request.

5. (Previously Presented) The method of claim 1, further comprising the step of determining a priority of the memory access request based upon a second identifier, in the event that the memory access request is speculative, and wherein the step of processing the memory access request comprises processing the memory access request, or not, based upon the conditions and the priority.

6. (Previously Presented) The method of claim 5, wherein the step of determining a priority comprises decoding the second identifier as a second bit field within the memory access request.

7. (Previously Presented) The method of claim 6, further comprising encoding the second bit field within the memory access request to define a priority of the memory access request.

8. (Previously Presented) The method of claim 1, wherein the memory access request comprises one of a memory read request and a memory load request.

9. (Previously Presented) The method of claim 1, wherein the step of determining comprises utilizing one of a CPU, chipset and memory controller to determine whether the memory access request is speculative.

10. (Previously Presented) The method of claim 9, wherein at least one of the CPU, chipset and memory controller independently controls the step of processing the memory access request based on the conditions.

11. (Original) The method of claim 1, wherein the step of assessing target resource conditions comprises assessing one or more of memory utilization, memory congestion, buffer space utilization, and bus congestion.

12. (Original) The method of claim 1, wherein the step of assessing interconnect conditions comprises assessing one or more of bus utilization, bus congestion, crossbar utilization, cross bar congestion, and point to point link utilization.

13. (Previously Presented) The method of claim 1, further comprising the step of notifying one or more logic devices when the memory access request is not processed.

14. (Previously Presented) In CPU architecture that initiates both speculative and non-speculative memory access requests, an improvement comprising decode logic for determining whether the memory access requests are speculative, and assessment logic for determining one or both of interconnect and target resource conditions, the CPU architecture processing speculative memory access requests, or not, as a function of the conditions.

15. (Previously Presented) In CPU architecture of claim 14, the further improvement comprising a prefetch unit for prefetching speculative

memory access requests, wherein the decode logic detects whether prefetched memory access requests are speculative.

16. (Previously Presented) A system for processing speculative memory access requests within a processing architecture, comprising: one or more memory access requests having a bit field defining the memory access requests as speculative or non-speculative; decode logic for decoding the bit field to determine whether one or more memory access requests are speculative; and processing logic for processing speculative memory access requests, or not, based on at least one of interconnect and target resource conditions.

17. (Previously Presented) A system of claim 16, one or both of the decode logic and processing logic being located within one of a CPU, a chipset, a bus controller or a memory controller.

18. (Previously Presented) A system of claim 16, wherein the memory access requests comprise memory read instructions.

19. (Original) A system of claim 16, further comprising a bus controller for assessing one or more of bus congestion and bus utilization conditions.

AF/3728

PTO/SB/31 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket Number (Optional): F1445-00

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]
on 4/1/05
Signature: Tracy Cavallaro
Typed or printed name: Tracy Cavallaro

In re Application of: Vesborg

Application Number	Filed
09/950,910	9/12/2001

For: Holographic Images

Art Unit	Examiner
3728	Pickett, John G.

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 500.00

- ☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $ _____
- ☐ A check in the amount of the fee is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☑ The Director has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.
- ☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 03-2455 . I have enclosed a duplicate copy of this sheet.
- ☑ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 39,425
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

Signature

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Telephone number

4/1/05
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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